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it may be injected through holes
k **30**.

wing FIG. **6** is shown with a
GA) of solder balls **72** on the
bstrate. Thus, the semiconductor
to another substrate such as a

of forming the semiconductor
and **6**, the gel elastomer layer **70**
18 of the semiconductor die **12**,
he attachment surface **46** of the

rawing FIGS. **5** and **6**, overpres-
interface is eliminated by the
l elastomer. Simultaneously, the
of the filled gel elastomer main-
from the device.

skilled in the art that various
may be made to the method and
n as disclosed herein without
and scope of the invention as
aims.

mbly comprising:
ace;
ng a plurality of edges, an active
e surface, the semiconductor die
e back side surface adhesively
of the substrate;
l covering a portion of the sur-
the plurality of edges of the
l a portion of the active surface
die; and
portion of the active surface of
.
sembly of claim **1**, wherein the
ty of fins thereon.
mbly comprising:
rality of circuits on a surface

ving a plurality of bond pads
rface thereof and having a back

connecting the plurality of bond
tor die to the plurality of circuits

4. The semiconductor assembly of claim **3**, wherein the heat sink cap includes a plurality of fins thereon.

5. The semiconductor assembly of claim **3**, wherein the compliant adhesive filled gel elastomer includes a cross-linked silicone.

6. A semiconductor assembly comprising:

a substrate having a plurality of electrical connections on a surface thereof;

at least one semiconductor die having a plurality of bond pads on an active surface thereof and having a back side surface, a portion of the back side surface adhesively attached to a portion of the surface of the substrate;

a plurality of wire bonds connecting the plurality of bond pads of the semiconductor die to the plurality of electrical connections of the substrate;

an encapsulant material covering a portion of the surface of the substrate, the plurality of bond pads on the active surface of the semiconductor die, a portion of the active surface of the semiconductor die, and the plurality of wire bonds; and

a heat sink attached to a portion of the active surface of the semiconductor die.

7. The semiconductor assembly of claim **6**, wherein the heat sink includes a plurality of fins thereon.

8. A semiconductor assembly comprising:

a substrate having a surface having a plurality of circuits thereon;

a semiconductor die having a plurality of bond pads located on an active surface thereof and having a back side surface;

a plurality of solder balls connecting the plurality of bond pads of the semiconductor die to the plurality of circuits of the substrate;

a metal filled cross-linked silicone compliant adhesive filled gel elastomer contacting a portion of the back side surface of the semiconductor die; and

a heat sink cap having a portion thereof in contact with a portion of the metal filled cross-linked silicone compliant adhesive filled gel elastomer, the heat sink cap enclosing the metal filled cross-linked silicone compliant adhesive filled gel elastomer, the semiconductor die, the plurality of solder balls, and at least a portion of the substrate.

9. The semiconductor assembly of claim **8**, wherein the heat sink cap includes a plurality of fins thereon.

* * * * *

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2x Patent + 103

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onto the top of the heat sink fins themselves.

(8) However, although heat sinks are effective in removing heat generated by a semiconductor die, attaching the heat sinks to the dies, or packages in a thermally efficient manner presents difficulties for semiconductor package designers. For example, FIG. 1B shows a cross-sectional view of a conventional encapsulated semiconductor package. The package 100 comprises a package substrate 102 having a plurality of solder balls 112 mounted to its lower surface. Solder balls 112 are used for providing electrical connection to a printed circuit board (not shown). A semiconductor die 106 is mounted to the upper surface of the package substrate 102 by a die attach material, such as epoxy, 114. Electrical connection between the circuit elements on the active surface of the die 106 and conductive traces on the package substrate 102 are provided by bond wires 108. An encapsulant 104 covers the die 106 and bond wires 108 in order to prevent damage to the package when it is handled and installed on the printed circuit board. This type of packaging is sometimes referred to as "glob-top" packaging due to the presence of the encapsulant 104. This type of packaging is desirable due to its low cost, however, the thermal performance of encapsulated packages are poor because the encapsulant 104 has a low thermal conductivity which prevents good heat transfer between the semiconductor die 106 and a heat sink which may be attached to the package.

(9) One solution to the above problem is to provide a direct connection between the heat sink and the semiconductor die. This can be accomplished by the use of "flip-chip" packaging. A cross-sectional view of a conventional flip-chip package is shown in FIG. 2. In this case, the package 200 includes a package substrate 202 having a number of electrically conductive solder balls 206 formed on its lower surface to provide electrical contact between the package 200 and a printed circuit board (not shown). A semiconductor die 210 is mounted to the upper surface of the package substrate 202 by a number of solder bumps 214 which are formed on bond pads on the active surface of the semiconductor die 210. An underfill material 212 is provided to encapsulate and protect the solder bumps 214. Thus, it is noted that unlike the encapsulated package shown in FIG. 1B where the active surface of the die faces away from the package substrate, in a flip-chip package the active surface of the die is "flipped" so that it faces the

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US006225695B1

(12) **United States Patent**
Chia et al.

(10) Patent No.: **US 6,225,695 B1**
(45) Date of Patent: ***May 1, 2001**

(54) GROOVED SEMICONDUCTOR DIE FOR FLIP-CHIP HEAT SINK ATTACHMENT

(75) Inventors: Chok J. Chia, Cupertino; Seng-Sooi Lim, San Jose; Maniam Alagaratnam, Cupertino, all of CA (US)

(73) Assignee: LSI Logic Corporation, Milpitas, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 08/869,796

(22) Filed: Jun. 6, 1997

(51) Int. Cl.⁷ .... [illegible]; H01L 23/34
(52) U.S. Cl. .... [illegible]; 257/707; 257/712; 257/706; 257/738; 257/737; 257/778; 257/713; 257/779; 257/782; 257/783
(58) Field of Search 257/712, 707, 257/710, 711, 723, 714, 717-722, 675, 686, 734, 737, 738, 706, 796, 778, 779, 782, 783

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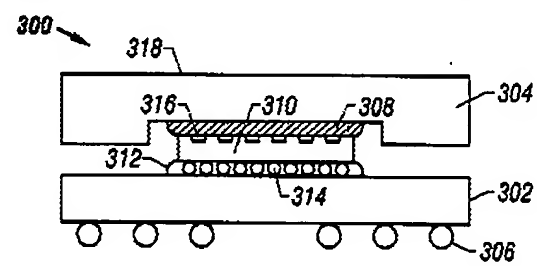
Primary Examiner—Alexander O. Williams

(57) ABSTRACT

One aspect of the invention relates to a flip-chip semiconductor package. In one version of the invention, the flip-chip semiconductor package includes a package substrate having an upper surface, a lower surface and a plurality of conductive traces, the upper surface having an upper plurality of electrical contacts coupled to the conductive traces, the lower surface having a lower plurality of electrical contacts coupled to the conductive traces, the lower plurality of electrical contacts being attachable to electrical contacts on a printed circuit board; a semiconductor die having an active surface and a non-active surface, the active surface having a plurality of circuit elements and a plurality of bond pads formed thereon, the bond pads being attached to the upper plurality of electrical contacts by solder bumps, the non-active surface having a plurality of grooves formed thereon; and a heat sink attached to the non-active surface of the semiconductor die.

16 Claims, 5 Drawing Sheets



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the heat sink 100 includes a base member 102, having a base surface 103 which is attachable to a corresponding surface of the semiconductor package. Heat sink 100 is also provided with a heat dissipating surface 105. In this case, the surface 105 includes fins 104a, 104b, 104c and 104d which provide greater surface area for convection cooling. Other designs include a plurality of cooling pins which rise from the base member. Numerous types of pins are known in the art having cross-sections of various shapes. Forced convection may be provided by a fan which passes air over a circuit board to which the packaged semiconductor is mounted, or, in some cases, a fan may be mounted directly onto the top of the heat sink fins themselves.

(8) However, although heat sinks are effective in removing heat generated by a semiconductor die, attaching the heat sinks to the dies, or packages in a thermally efficient manner presents difficulties for semiconductor package designers. For example, FIG. 1B shows a cross-sectional view of a conventional encapsulated semiconductor package. The package 100 comprises a package substrate 102 having a plurality of solder balls 112 mounted to its lower surface. Solder balls 112 are used for providing electrical connection to a printed circuit board (not shown). A semiconductor die 106 is mounted to the upper surface of the package substrate 102 by a die attach material, such as epoxy, 114. Electrical connection between the circuit elements on the active surface of the die 106 and conductive traces on the package substrate 102 are provided by bond wires 108. An encapsulant 104 covers the die 106 and bond wires 108 in order to prevent damage to the package when it is handled and installed on the printed circuit board. This type of packaging is sometimes referred to as "glob-top" packaging due to the presence of the encapsulant 104. This type of packaging is desirable due to its low cost, however, the thermal performance of encapsulated packages are poor because the encapsulant 104 has a low thermal conductivity which prevents good heat transfer between the semiconductor die 106 and a heat sink which may be attached to the package.

(9) One solution to the above problem is to provide a direct connection between the heat sink and the semiconductor die. This can be accomplished by the use of "flip-chip" packaging. A cross-sectional view of a conventional flip-chip package is shown in FIG. 2. In this case, the package 200 includes a package substrate 202 having a number of

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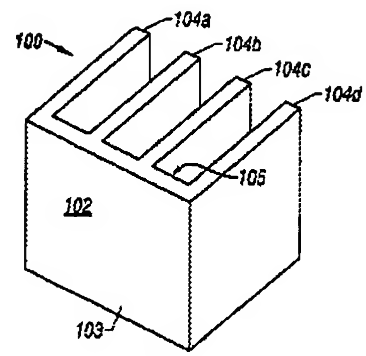

FIG. 1A
(Prior Art)

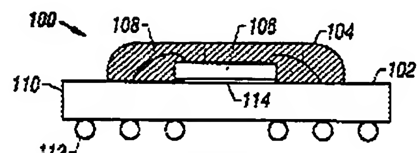

FIG. 1B
(Prior Art)

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US005909056A

United States Patent [19]

Mertol

[11] Patent Number: 5,909,056

[45] Date of Patent: Jun. 1, 1999

[54] HIGH PERFORMANCE HEAT SPREADER FOR FLIP CHIP PACKAGES

[75] Inventor: Atila Mertol, Cupertino, Calif.

[73] Assignee: LSI Logic Corporation, Milpitas, Calif.

[21] Appl. No.: 08/868,316

[22] Filed: Jun. 3, 1997

[51] Int. Cl.[6] H05K 7/20; H01L 23/02

[52] U.S. Cl. 257/706; 257/712; 257/717; 257/737; 257/738; 257/787; 257/707; 257/796; 257/722; 438/122; 438/121; 361/383

[58] Field of Search 257/712, 706, 257/717, 720, 675, 796, 738, 707, 734, 710, 713, 721, 787, 795; 361/707, 714, 719; 174/16.3; 438/122, 121

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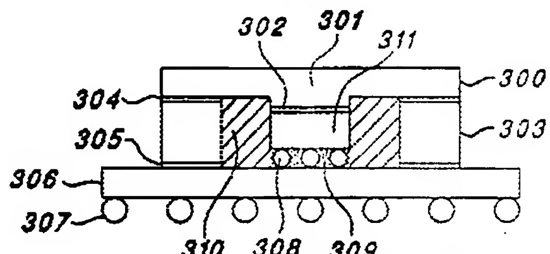
Primary Examiner—Alexander Oscar Williams

[57] ABSTRACT

According to one aspect of the invention, a semiconductor package is provided including a package substrate having an upper surface and a lower surface, wherein electrical contacts on the lower surface of the substrate are coupled to corresponding electrical contacts on a printed circuit board by a plurality of solder balls; a semiconductor die having a non-active surface and an active surface, wherein the active surface is electrically coupled to the upper surface of the package substrate by a plurality of solder bumps; and an integrated heat spreader and ring stiffener coupled with the non-active surface of the semiconductor die by a phase change material which is retained by a miniature dam ring while in a liquid state, wherein heat generated by the die is transferred to the heat spreader, and wherein the heat spreader has a protrusion formed thereon which matches the outermost size of the die.

1 Claim, 1 Drawing Sheet



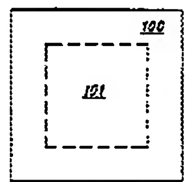


FIG. 1A

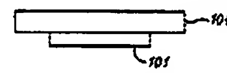


FIG. 1B

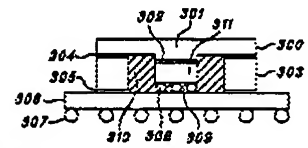


FIG. 3

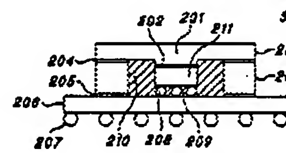


FIG. 2

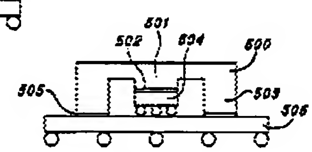


FIG. 5

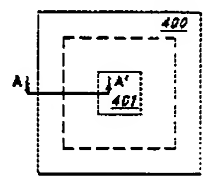


FIG. 4A

FIG. 4B

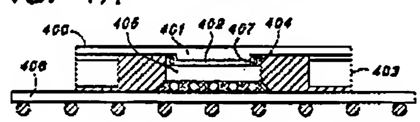


FIG. 4C

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Thus, the thermal conductivity of the thermally conductive elastomer limits the overall ability to dissipate ohmic heat.

(5) Typical thermally conductive elastomers contain a ceramic filler such as boron nitride or alumina in an elastomer matrix. The alumina is generally in the form of irregularly shaped .alpha.-alumina particles. The elastomers used are usually urethane or silicone based. While these materials are adequate in many instances, there is a constant demand for thermally conductive elastomers with improved thermal conductivity and electrical insulating properties.

(6) SUMMARY OF THE INVENTION

(7) The invention provides filled thermally conductive electrically insulating elastomers of improved thermal conductivity using alumina platelets as the filler.

(8) In one aspect, the invention encompasses a thermally conductive electrically insulating filled elastomer composition comprising an elastomer and filler, the filler comprising alpha alumina platelets.

(9) The platelets preferably average less than one micron in thickness and preferably have an average aspect ratio of at least about 5:1. Preferably the elastomer composition contains at least about 70 wt% alumina platelets.

(10) DETAILED DESCRIPTION OF THE INVENTION

(11) The compositions of the invention generally comprise an elastomer and alpha alumina platelets as a thermally conductive filler.

(12) The elastomer may be any known compatible elastomer such as silicones, styrene-containing block copolymers, olefin-containing block copolymers, and the like. The elastomer may be a crosslinkable block copolymer if desired.

(13) Silicone elastomers are preferably formed from a silicone gum which is crosslinked using a catalyst. An example of a suitable silicone gum is sold under the name "Silastic.RTM. 4-2765" by Dow Corning, Inc. A peroxide catalyst: 2,5-dimethyl 2,5-bis (t-butyl peroxy) hexane 50% on CaC0.sub.3 sold by R. T. Vanderbilt as Varox.RTM. DBPH-50 is an example of a suitable catalyst.

(14) Preferred block copolymers are thermoplastic rubbers such as Kraton.RTM.

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THERMALLY CONDUCTIVE ELASTOMER CONTAINING ALUMINA PLATELETS

BACKGROUND OF THE INVENTION

Thermally conductive elastomers are elastomeric materials which contain a thermally conductive filler. They are primarily used in electronics applications in instances where good thermal conduction and electrical insulation are needed in the same material. For example, a thermally conductive elastomer may be used as an interface between a semiconductor electronic component and a metal heat sink.

Many electronics designs and applications are linked by the ability to dissipate ohmic heat generated during the operation of the electronics. Many electronic components, especially semiconductor components, are prone to breakdown at high temperatures. Thus, the ability to dissipate heat is a limiting factor on the performance of the component.

High thermal conductivity metal heat sinks, because of their high electrical conductivity, cannot be directly contacted with electronic components. Therefore, thermally conductive elastomer material is used as a thermally conductive, electrically insulating interface between the electronic component and the metal heat sink. The thermal conductivity of thermally conductive elastomer is generally much less than that of the metal heat sink. Thus, the thermal conductivity of the thermally conductive elastomer limits the overall ability to dissipate ohmic heat.

Typical thermally conductive elastomers contain a ceramic filler such as boron nitride or alumina in an elastomer matrix. The alumina is generally in the form of irregularly shaped α-alumina particles. The elastomers used are usually urethane or silicone based. While these materials are adequate in many instances, there is a constant demand for thermally conductive elastomers with improved thermal conductivity and electrical insulating properties.

SUMMARY OF THE INVENTION

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Silicone elastomers are preferably formed from a silicone gum which is crosslinked using a catalyst. An example of a suitable silicone gum is sold under the name "Silastic® 4-2765" by Dow Corning, Inc. A

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